

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:)
Brox et al.)
)
MMB Docket No. **1890-0030**) Examiner: **To be assigned**
)
Application No. **To be assigned**) Group Art Unit: **To be assigned**
)
Filed: **Herewith**)
)
For: **Delay Locked Loop and a Method for Delay Control**

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Harold C. Moore

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Signature

December 30, 2003

Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicant hereby discloses the following references, copies of which are enclosed, regarding the above-identified patent application.

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
5,604,775	February 18, 1997	Saitoh et al.
6,326,826	December 4, 2001	Lee et al.
<u>Foreign Application</u>	<u>Issue Date</u>	<u>Country</u>
DE 19930167 A1	January 18, 2001	Germany

Articles

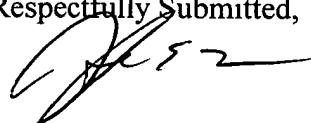
Atsushi Hatakeyama et al. "A 256-Mb SDRAM Using a Register Controlled Digital DLL," IEEE Journal of Solid-State Circuits, Vol 32, No 11, ©1997, pages 1728-1734, (7 pages).

The above-identified documents were cited in a German Office Action (copy enclosed) in a related German patent application number 10261409.1-35 filed on December 30, 2002. It is believed no translation of the German patent (DE 19930167 A1) is needed.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

December 30, 2003
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Respectfully Submitted,



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FORM PTO-1449 <u>INFORMATION DISCLOSURE STATEMENT</u>	MMB DOCKET NO. 1890-0030	APPLICATION NO.: To be assigned
	APPLICANT(S): Brox et al.	
	FILING DATE: Herewith	GROUP ART UNIT: To be assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	5,604,775	February 18, 1997	Saitoh et al.			
	AB	6,326,826	December 4, 2001	Lee et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	DE 19930167 A1	January 18, 2001	Germany			Yes No
	AM						Yes No
	AN						Yes No
	AO						Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AQ	1	Atsushi Hatakeyama et al. "A 256-Mb SDRAM Using a Register Controlled Digital DLL," IEEE Journal of Solid-State Circuits, Vol 32, No 11, ©1997, pages 1728-1734, (7 pages).
AR	1	
AS	1	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.